REMARKS

Applicants appreciate the courtesy of Examiner Zaidi conducting a telephone interview with Applicants' representative on March 19, 2008. During the interview, Applicants' representative discussed the claimed invention and the amended claims provided herein. The Examiner agreed that the amended claims would overcome the prior art of record.

Claims 1-17 are pending in the application. Independent claims 1, 11, and 12 have been amended to further define the claimed "data clock" and to recite that an adjusting signal is produced based on a phase difference between a clock of a frame transmission and the data clock (see independent claim 1; *see also* claims 11 and 12). The amendments are fully supported by the application as originally filed (see specification at page 1, lines 32-34; page 11, lines 20-34).

For example, as recited in independent claim 1, a method for controlling a phase of successively transmitted frames includes steps of: "determining a phase difference between a clock of a frame transmission and a data clock corresponding to the frequency at which the data symbols are transmitted"; and "producing an adjusting signal based on the determined phase difference in order to control an injection of stuffing data symbols into the frames..." (see independent claim 1; specification at page 1, lines 32-34; and page 11, lines 20-34).

Claims 1-14 and 16 were rejected under 35 USC 102(b) as being anticipated by U.S. Patent 5,708,684 to Ueda. Claims 15 and 17 were rejected under 35 USC 103(a) as being unpatentable over Ueda in view of U.S. Patent 4,392,220 to Hirosaki et al. These rejections are respectfully traversed.

Regarding the rejection of independent claims 1, 11, and 12 over Ueda, the Ueda reference does not teach or suggest at least determining a phase difference between (1) a clock of a frame transmission, and (2) a data clock "corresponding to the frequency at which the data symbols are transmitted"; or where an adjusting signal is produced based on the determined phase difference in order to control an injection of stuffing data symbols into the frames, as recited in independent claim 1 (*see also* claims 11 and 12).

Referring to FIG. 5 of Ueda, e.g., two clock signals are compared in a clock phase comparator, and two data signals are compared in a data phase comparator.

However, there is no teaching or suggestion in Ueda that a phase difference is determined between (1) a clock of a frame transmission, and (2) a data clock "corresponding to the frequency at which the data symbols are transmitted," as claimed.

Further, there is no teaching or suggestion in Ueda that an adjusting signal is produced based on the determined phase difference in order to control an injection of stuffing data symbols into the frames, as claimed.

Referring to column 1, line 54 to column 2, line 7 of Ueda, prior art radio equipment is described in which stuffing bits are inserted "in accordance with the difference in the data input rate and the data output rate" (column 1, lines 54-56 of Ueda).

However, there is no teaching or suggestion in Ueda that the stuffing bit insertion disclosed with respect to the prior art is controlled by an adjusting signal produced based on a phase difference between (1) a clock of a frame transmission, and (2) a data clock, as claimed.

It is believed that the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

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